

COA (BCA -303) Unit Test paper

* Required

1. Email address *

2. Class *

3. Roll Number *

4. The collection of paths connecting the various modules is call the Interconnection Structure *

Mark only one oval.

☐ True

☐ False

5. What is the step during which a new instruction is read from the memory? *

Mark only one oval.

☐ Fetch

☐ Decode

☐ Execute

☐ None of these

6. The instruction includes the following fields:

Mark only one oval.

- ☐ Opcode
- ☐ Operand
- ☐ Mode
- ☐ All of the above

7. Interrupts are provided to improve the Execution efficiency of the processor

Mark only one oval.

- ☐ True
- ☐ False

8. Arithmetic overflow, Division by zero are examples of _____ Interrupt

Mark only one oval.

- ☐ Timer
- ☐ Program
- ☐ Input/Output
- ☐ Hardware Failure

9. Bus lines permanently assigned to only one function is known as

Mark only one oval.

- ☐ Dedicated Bus
- ☐ Multiplexed Bus
- ☐ Synchronous Bus
- ☐ None of the above

10. How does the CPU handle Multiple Interrupts?

Mark only one oval.

- ☐ Disable Interrupts
- ☐ Define Priorities
- ☐ Both
- ☐ None of the Above

11. The iac in the Instruction cycle state diagram refers to _____

Mark only one oval.

- ☐ Instruction Operation Decoding
- ☐ Instruction Address Calculation
- ☐ Instruction Fetch
- ☐ None of the above

12. The Asynchronous bus is based on the use of Handshaking signals

Mark only one oval.

- ☐ True
- ☐ False

13. The If, Of, Os instruction cycle states refer to the communication between CPU & memory or I/O module

Mark only one oval.

- ☐ True
- ☐ False

14. The Register which includes the address of the memory unit is _____ *

Mark only one oval.

- ☐ IR
- ☐ MAR
- ☐ PC
- ☐ None of these

15. _____ is the sequence of operations performed by a CPU in processing an instruction *

Mark only one oval.

- ☐ Execute cycle
- ☐ Decode
- ☐ Fetch
- ☐ Instruction Cycle

16. The CPU consists of General purpose & Special purpose registers *

Mark only one oval.

- ☐ True
- ☐ False

17. Which of the following are the features of a Distributed Arbitration method? *

Mark only one oval.

- ☐ There is no Central Controller
- ☐ Code for Access Control on all modules
- ☐ Modules act together to share the bus
- ☐ All of the above

18. _____ keeps a track of the execution of a program *

Mark only one oval.

- ☐ IR
- ☐ PC
- ☐ MDR
- ☐ MAR

19. Computer Organization refers to the operational units and their interconnections that realize the architectural specifications *

Mark only one oval.

- ☐ True
- ☐ False

20. Memory module has the following types of exchanges for interconnection with other units *

Mark only one oval.

- ☐ Read
- ☐ Write
- ☐ Address
- ☐ All of these

21. An I/O module may control more than one external device. *

Mark only one oval.

- ☐ True
- ☐ False

22. An I/O module is allowed to exchange data directly with memory, without going through the processor. This is known as _____ *

Mark only one oval.

- ☐ Internal Data
- ☐ External Data
- ☐ Direct Memory Access
- ☐ None of the above

23. Only a single transmission is possible at a time on a Bus *

Mark only one oval.

- ☐ True
- ☐ False

24. When several lines are used to transmit bits simultaneously, it is called _____ transmission *

Mark only one oval.

- ☐ Serial
- ☐ Parallel
- ☐ None of the above

25. A bus that connects major components (CPU, Memory, I/O) is called _____ Bus *

Mark only one oval.

- ☐ Address
- ☐ System
- ☐ Data
- ☐ None of the above

26. _____ Bus is Unidirectional *

Mark only one oval.

- ☐ Data
- ☐ System
- ☐ Address
- ☐ Control

27. The width of the Data bus determines the _____ of the computer system *

Mark only one oval.

- ☐ Overall performance
- ☐ Memory capacity
- ☐ None of the above

28. Control signals transmit both command & timing information between memory, I/O , etc. *

Mark only one oval.

- ☐ True
- ☐ False

This content is neither created nor endorsed by Google.

Google Forms